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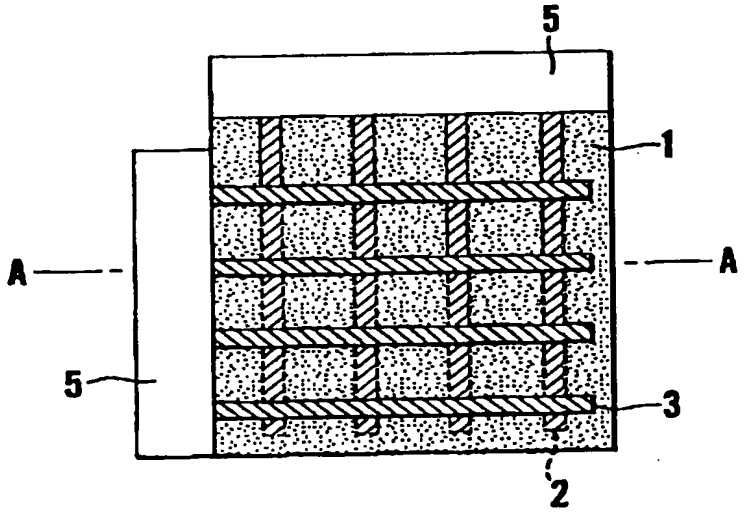
(57) Abstract

In a ferroelectric data processing device for processing and/or storage of data with passive or electrical addressing a data–carrying medium is used in the form of a thin film (1) of ferroelectric material which by an applied electric field is polarized to determined polarization states or switched between these and is provided as a continuous layer in or adjacent to electrode structures in the form of a matrix. A logic element (4) is formed at the intersection between an x electrode (2) and a y electrode (3) of the electrode matrix. The logic element (4) is addressed by applying to the electrodes (2, 3) a voltage greater than the coercivity field of the ferroelectric material. Dependent on the polarization state and the form of the hysteresis loop of the ferroelectric material a distinct detection of the polarization state in the logic element (4) is obtained and it may also be possible to switch between the polarization states of the logic element, which hence may be used for implementing a bistable switch or a memory cell. The data processing device according to the invention may be stacked layerwise if the separate layers are separated by an electrical isolating layer and hence be used for implementing volumetric data processing devices.



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A ferroelectric data processing device

The present invention concerns a ferroelectric data processing device, particularly for processing and/or storage of data with active or passive electrical addressing, comprising a data-carrying medium in the form of a thin film of ferroelectric material, wherein the ferroelectric material by an applied electric field may attain a first or a second polarization state by being switched from a disordered state to one of the polarization states or from the first to the second polarization state or vice versa, wherein the ferroelectric material comprises logic elements, and wherein a polarization state assigned to a logic element represents a logical value of the logic element

The present invention also concerns a method for manufacturing an embodiment of the ferroelectric data processing device, as well as a method for addressing of logic elements in a ferroelectric data processing device, wherein the logic elements are provided in an electrical connected passive matrix, particularly for processing and/or storage of data with active or passive electrical addressing, depending on whether an addressing operation causes a change in a polarization state possibly already present in the logic element, comprising a data-carrying medium in the form of a thin film of a ferroelectric material, wherein the ferroelectric thin film by an applied electrical field may attain a first or second polarization state and is switched from a disordered state to one of the polarization states or from the first to the second polarization state or vice versa, wherein the ferroelectric thin film is provided as a continuous layer in or adjacent to respectively a first or second electrode structure and comprises the logic elements which contact electrodes in this first and second electrode structure, wherein a polarization state assigned to a logic element represents the logical value of the logic element, and wherein the addressing comprises steps for writing, reading, erasing and switching of data in the logic element.

Generally the invention concerns data processing devices with logic elements implemented in a ferroelectric material. The phenomena of ferroelectricity is in this connection supposed known by persons skilled in the art, as the field is comprehensively treated in the literature, for instance in J.M. Herbert, Ferroelectric Transducers and Sensors, Gordon and Breach, 1982, wherein in pp. 126-130 there is proposed using a ferroelectric memory based on single crystals of barium titanate provided between orthogonal electrodes in an x,y electrode matrix. The author concludes that there are substantial practical

difficulties connected with the use of ferroelectric single crystals for information storage in this simple manner. In regard of recent survey literature, reference may be made to R.G. Kepler and R.A. Anderson, Advances in Physics, Vol. 41, No. 1, pp. 1-57 (1992).

As mentioned above, the data-carrying medium is a ferroelectric material in the form of thin film. Such ferroelectric thin films which either may be inorganic, ceramic materials, polymers or liquid crystals have been known for some time and it may in this connection be referred to the above-mentioned article by Kepler and Anderson. There are for instance from J.F. Scott, Ferroelectric memories, Physics World, February 1995, pp. 46-50, known data storage devices based on ferroelectric memory materials. They all have in common that at least one transistor is necessary in each bit location or memory cell. In the most common embodiments the ferroelectric material is used as a dielectric in the associated memory circuit and comprises a bit-storing capacitor. Due to the high dielectric constant of ferroelectric materials, the capacitor may be made much smaller than otherwise possible and will additionally provide a quite superior charge lifetime. Recently the development has focused on another property of ferroelectric materials, namely their ability to be polarized electrically when they briefly are subjected to a strong electric field. During the polarization process the dipoles of the ferroelectric material attains a preferred orientation, something which results in a macroscopic dipole moment which is retained after the removal of the polarizing field. By thus including the ferroelectric material in the gate electrode structure of a field effect transistor in the memory cell circuit, the transconductance characteristics of the transistors may be controlled by controlling the polarization state of the ferroelectric material. The latter may be switched, for instance by polarizing fields with a direction which either causes a transconductant state "on" or "off" in the transistor.

EP patent 0 721 189 discloses a ferroelectric memory with discrete memory cells provided in an electrode matrix. In addition to a discrete ferroelectric capacitor each memory cell also comprises switching means, preferably in the form of at least one transistor. The discrete memory cells hence do not form a passive matrix. With discrete memory cells it shall here be understood that the ferroelectric capacitor is formed by a discrete component, such that the ferroelectric material cannot form a continuous layer in the matrix. There are provided separate data and selection lines and the read-out of a stored datum may take place in current or voltage mode on data lines provided for this

purpose, but according to a relatively complicated protocol, such as disclosed by patent claim 6. It must also be remarked that the number of memory cells connected in a data signal line must be adjusted in order to adjust parasitic capacitance on each data signal line during the readout, such that the voltage variation on one of the data signal lines is minimized.

US patent 5 592 409 concerns a non-volatile ferroelectric memory wherein data may be read out without destruction. The memory cells are included in an active matrix and are formed as transistor structures therein, wherein the gate electrode makes one of the electrodes in a ferroelectric capacitor. It is evident that the ferroelectric capacitors are discrete components. The polarization of the capacitor takes place in an as per se well-known manner, but by the read-out which takes place in current mode it is the drain current that is detected, this in order to prevent the stored data from being erased.

Even if the use of ferroelectric materials as mentioned above represents substantial improvements relative to alternative technologies for storage of data, the basic architecture of ferroelectrically based memories is directed to the use of active microcircuits included in each memory cell. This has negative consequences for the achievable data storage density, i.e. the number of bits which may be stored on a given surface area, as well as for the cost for each bit stored, something which partly may be due to complicated manufacturing technology and the use of active semiconductive components.

It has also been shown that ferroelectric polymer materials may be used in erasable optical memories. M. Date & al. has in the paper "Opto-ferroelectric Memories using Vinylidene Fluoride and Trifluoroethylene Copolymers", IEEE Trans. Electr. Ins., Vol. 24, No. 3, June 1989, pp. 537-540, proposed a data medium comprising a dye-doped vinylidene fluoride trifluoroethylene copolymer with a thickness of 2μm, spin deposited on a ITO coated glass plate. The information is written as sequences of positive and negative polarizations generated by irradiating with a focused laser beam with a diameter of about 5 μm in the presence of sign controlling electric fields. The data is read out pyroelectrically by scanning with a laser beam. A carrier/noise ratio of 48 dB has been obtained by using a regularly repeating data train in the form of 0/1-state with a pitch of 20 μm and with the use of a laser power of 12 mW and field strength of 25 MV/m. The reading speed was then 100 mm/s.

The object of the present invention is to provide a simple logic architecture which may be used for realising either bistable switches or memory cells in a data processing device or to provide a purely ferroelectric data storage device which offers the possibility of storing a very high number of bits in an area unit and which at the same time may be produced in simple manner in high volume with low cost, such that the above-mentioned disadvantages of the prior art are avoided.

This object is achieved according to the invention with a ferroelectric data processing device which is characterized in that the ferroelectric thin film is provided as a continuous layer in or adjacent to respectively a first and second electrode structure, that the first and the second electrode structure each comprises substantially mutually parallel strip-like electrodes, such that the electrode structures mutually form a substantially orthogonal x,y matrix, wherein the electrodes in the first electrode structure constitute the columns of the electrode matrix or the x electrodes and the electrodes in the second electrode structure the rows of the electrode matrix or y electrodes, and that a portion of the ferroelectric thin film at the intersection between an x electrode and a y electrode of the electrode matrix forms a logic element such that the logic elements jointly form an electrically connected passive matrix in the data processing device; a method for manufacturing of a ferroelectric data processing device being characterized by successive steps for depositing a first electrode structure on a substrate, depositing a layer of electrical isolating material over the first electrode structure, depositing a second electrode structure over the isolating layer, removing the isolating layer where it is not covered by the second electrode structure, such that the electrodes in the first electrode structure is exposed except in the intersection between the electrodes of respectively the first and the second electrode structure, and depositing a ferroelectric thin film in the form of a continuous layer over the electrode structures; and a method for addressing a ferroelectric data processing device, being characterized by the step for writing comprising applying a voltage to the logic element and polarizing the ferroelectric thin film of the logic element to a positive or a negative polarization state which respectively corresponds to a logical 0 or a logical 1 or vice versa, by the step for reading comprising applying a voltage to a logic element and detecting the charge transfer between the electrodes in the logic element in the form of a current value, which uniquely indicates the logical value, by the step for erasing comprising applying to all logic elements in the data processing device a voltage which

gives all logic elements one and the same polarization state, and by the step for switching of a logic element from a polarization state which corresponds to a logical 0 or a logical 1 or vice versa, comprising applying a voltage to the logic element which reverses the initial polarization state of the logic element.

According to the invention the ferroelectric thin film is advantageously formed of a ceramic material or a ferroelectric liquid crystal material or a polymer or copolymer, the copolymer preferably being a vinylidene fluoride/trifluoroethylene copolymer.

According to the invention in one embodiment the ferroelectric thin film is preferably provided between the first and the second electrode structure and the logic element is formed in the intersection between an x electrode and a y electrode.

According to the invention in another embodiment a layer of electrical isolating material is preferably provided between and adjacent to the electrodes of the first and the second electrode structure, the ferroelectric thin film being provided in the form of a continuous layer over the electrode structures on one side thereof and the logic elements are formed respectively in a portion of the ferroelectric thin film at the side edges of a y electrode at the intersection between the x electrode and the y electrode.

In the method for manufacture of the ferroelectric data processing device it is according to the invention advantageous that the substrate is formed of a crystalline, polycrystalline or amorphous semiconducting material. for instance silicon.

In the method for addressing of a data processing device according to the invention it is particularly preferred applying a voltage which between the electrodes of the logic element generates a field strength which is more than twice the coercivity field of the ferroelectric material. According to the invention it is preferred that the current detection in the reading step takes place either by sampling in the time domain or in a time window dependent on the saturation time constant of the polarization. Advantageously the current detection, particularly in the latter case, takes place by a level comparison.

It is according to the invention also preferred that the current detection in the reading step is verified in an immediate following step by applying to the logic element a voltage corresponding to the voltage used in the reading step. but of

opposite polarity, and by detecting the charge transfer between the electrodes in the logic element in the form of a current value.

If the step for reading and/or verification causes a destruction of a datum stored in the logic element, it is according to the invention preferred that the logic element is reset to its initial logic state after the current detection in the step for reading or verification by applying to the logic element a voltage which restores the initial polarization state of the logic element.

Further features and advantages will be evident from the additional appended dependent claims.

The invention shall now be explained in a more detail in connection with examples of embodiments of both the data processing device and the method and with reference to the accompanying drawing, wherein

fig. 1 shows a first embodiment of a ferroelectric data processing device according to the invention, seen in plan view,

fig. 2 the data processing device in fig. 1 in a schematic section taken along the line A-A in fig. 1,

fig. 3a a plan view of a logic element in the data processing device in fig. 1,

fig. 3b schematically the polarization of the logic element in fig. 3a.

fig. 4 a second embodiment of the data processing device according to the invention, seen in plan view,

fig.5 the data processing device in fig. 4 in a schematic section taken along line A-A in fig. 4,

fig. 6a a plan view of a logic element in the data processing device in fig. 4,

fig. 6b schematically the polarization of the logic element in the data processing device in fig. 3,

fig. 7 a typical hysteresis loop for the polarization of a ferroelectric copolymer material,

fig. 8 a diagram of the time response of a detected output signal,

fig. 9 a diagram of the switching characteristics of a ferroelectric copolymer material,

fig. 10 schematically and in perspective the embodiment of the data processing device in fig. 1 as an x,y electrode matrix with x=y=5, and

fig. 11 the data processing device corresponding to that in fig. 10 and arranged in stacked layers in order to implement a volumetric configuration.

In the following examples of embodiments of the ferroelectric data processing device shall be disclosed in connection with data processing devices with the logic element configured as memory cells, i.e. the device in its entirety implementing a data storing device. Similarly there shall in the following only be referred to the use of passive electric addressing of the individual logic element.

Fig. 1 shows a data storage device with a ferroelectric thin film 1 provided between a first and a second electrode structure. The first and the second electrode structure form as shown in the plan view in fig. 1 a two-dimensional x,y-matrix with the electrodes 2 of the first electrode structure as columns in the matrix or x electrodes and the electrodes 3 in the second electrode structure as rows in the matrix or y electrodes. Electrodes 2, 3 are connected to respective driver and control circuits 5 for driving the electrodes and detection of output signals.

The electrodes 2,3 and the ferroelectric thin film are as shown in section in fig. 2 taken along the line A-A in fig. 1, provided in sandwich configuration between a not shown overlying and underlying substrate which for instance may consist of crystalline silicon. The substrates are for the sake of clarity also left out in fig. 1. Between the respective substrates and the electrodes 2. 3 and the ferroelectric thin film 1 there may be provided not shown layers of electrical isolating material. As the substrates themselves have been made in semiconductor material, the driver and control circuits 5 may advantageously be made integrated with the substrates in a compatible technology, for instance along a side edge of the data processing device as suggested.

Fig. 3a renders enlarged the intersection between an x electrode 2 and a y electrode 3 as well as the active area 4 which contitutes a logic element in the ferroelectric thin film 1. This active area 4 will, when applying to the electrodes 2. 3 a drive voltage which generates an electric field between the x electrode and the y electrode 3, be polarized electrically in a direction which is determined by the sign of the drive voltage or the polarization voltage. The logic element 4 with the active area in the ferroelectric thin film 1 between the

electrodes 2, 3, is taken along the line B-B in fig. 3a, shown schematically in polarized state in fig. 3b which implies a polarization in the direction "up" which for instance may correspond to the positive polarization and hence represent a state logic 0 and logic 1 in the logical element 4 or in the memory cell formed in the volume of the ferroelectric thin film 1 in the intersection between the x electrode 2 and the y electrode 3. The detection of the polarization state, i.e. whether it is positive or negative, may now quite simply take place by passively addressing the logic element 4 with a voltage and by detecting the polarization state as representative for a determined logic state in the logic element 4 by the charge transfer between the electrodes 2, 3 during the addressing, hence in current mode. The output signal is registered by the control circuits and corresponds to the reading of the logical value assigned to the logic element 4 or memory cell by its present polarization state. This shall, however, be discussed in more detail in connection with the following description of the method for addressing.

Another embodiment of the data processing device according to the invention is shown in fig. 4. Herein the electrode structures are realized in a bridge configuration which, however, is known from NO patent application 973390, filed 17 June 1997 and assigned to the present applicant. As before. the electrodes 2; 3 in each structure are provided above each other in a matrix-like configuration and between not shown substrates which once again may be of crystalline silicon, as it is shown by the section in fig. 5 which is taken along the line A-A in fig. 4. In contrast with the preceding embodiment the ferroelectric thin film 1, however, is provided over the electrode structures. The electrodes 2 of the first electrode structure are electrically isolated from the electrodes 3 in the second electrode structure by providing a layer 6 of electrical isolating material in the intersection between the electrodes 2, 3. The active area in the ferroelectric thin film 1 and which comprises the logic element 4 itself, will thus appear as shown in plan view in fig. 6a and in section shown in fig. 6b taken along the line B-B in fig. 6a. In fig. 6b also the polarization of the active area is shown for a corresponding polarization as in fig. 3b, but with the field lines curved along the side edges of the isolation layer in the active area. The drive and control circuits may be realized in semiconductor technology and provided in the not shown semiconductor substrate or as separate circuit modules 5 provided along the side edges of the matrix as disclosed by fig. 4 and 5.

In the manufacturing of the embodiment shown in figs. 4 and 5 the first electrode structure is deposited on a substrate and then covered by an isolating layer 6. On the top of the isolating layer 6 the second electrode structure is now deposited, such that the first and the second electrode structure once again form a two-dimensional matrix configuration wherein the x electrodes 2 are the columns and the y electrode 3 the rows. In the areas where the isolating layer 6 is not covered by the electrodes 3 in the second electrode structure, the isolating material is now etched away, such that the electrodes 2 in the first electrode structure still are completely electrically isolated from the electrodes 3 of the second electrode structure at the intersection of the electrodes, but else exposed. The ferroelectric thin film 1 is now provided over the electrode structures before all parts possibly also are covered by an overlying substrate. Otherwise the embodiment is wholly similar to that shown for the data processing device in fig. 1 and 2. One advantage of the embodiment in fig. 4 and 5 is that the electrode structures and the accompanying connections and driver and control circuits are provided on for instance crystalline silicon substrates before the ferroelectric thin film is applied. Hence the different process steps which are included in the manufacturing of the active circuit elements in semiconductor technology may be performed without disturbing the ferroelectric thin film which for instance may be a polymer with a limited temperature tolerance.

There are a number of ferroelectric materials which may be used in the ferroelectric thin film. The ferroelectric material may e.g. be an inorganic ceramic material as lead zirconate titanate, a ferroelectric liquid crystal material or thin films of polymers. One instance of the latter is a copolymer of vinylidene fluoride (called VF2 or VDF) and trifluoroethylene (C_2F_3H, called TFE) where the relative content of each component in thin film may be varied in order to obtain different properties. Such copolymers may typically have a low coercivity field and show a more square hysteresis loop than which is the case for pure vinylidene fluoride polymers.

The switching characteristics of ferroelectric polymers realized as vinylidene flouride/triflouroethylene copolymers are discussed in a paper by Y. Tajitsu & al. with the title "Investigation of Switching Characteristics of Vinylidene Fluoride/Triflouroethylene Copolymers in Relation to Their Structures", (Japanese Journal of Applied Physics. 26, pp. 554-560 (1987)) and shall be regarded as a general reference in connection with the following description of

the addressing of a logic element or a memory cell in the data processing device according to the invention.

Fig. 7 shows the hysteresis loop for the polarization of a ferroelectric thin film for instance made of vinylidene fluoride/trifluoroethylene copolymer.

Polarization in C/m^2 is shown on the y axis and the interelectrode field strength in V/m on the x-axis. The ferroelectric thin film between the electrodes will initially be in a disordered or unpolarized state and be polarized when applying to the electrodes a voltage which generates a field strength between electrodes greater than the coercivity field of the ferroelectric material. The ferroelectric material will dependent on the sign of the polarization voltage attain an electric polarization with preferred orientation "up" represented by the point I or the hysteresis loop or "down" represented by point II on the hysteresis loop. The polarization states I and II may also be used to represent a logic 0 or a logic 1 or vice versa. It shall be remarked that the concepts "positive", "negative", "up", "down" of course, must be regarded as conventionally normative, as they are determined as soon as a determination has been made as to what shall be regarded as the positive or negative electrode or the polarization "up" or the polarization "down". A corresponding convention will be valid for the choice of which polarization state which shall be regarded as logical 1 or logical 0, and this should not lead to problems provided a determined protocol is strictly adhered to.

Consequently a logic element of a ferroelectric material which are in one of two polarization stages may represent a logic 0 or 1 or a binary 0 or 1 and be implemented as either bistable switches in a data processing device or memory cells in a data storing device. The polarization of the logic element to a determined state represent in other words writing of data to this logic element.

It may be mentioned that the polarization of suitable ferroelectric materials used in a logic element may take place at room temperature and with high speed by choice of suitable ferroelectric materials and the use of a correspondingly high field strength by the polarization voltage applied to the electrodes of the logic element. When the ferroelectric material is provided as a thin film, this comports a number of advantages. As soon as the logic element, i.e. the ferroelectric thin film material in the logic element has been given a preferred polarization, this polarization state will last for an indefinite

time period at room temperature and in any case for many years unless the polarization state is reversed by using a polarization field with opposite sign. A cancellation of the polarization state may take place in analogy with ferromagnetic demagnetization by running the logic element through a cyclic depolarization field. Strong heating of the logic element also may lead to a destruction of the polarization state by the electric dipoles loosing their preferred orientation.

The polarization direction along the hysteresis loop when applying a polarization field is indicated with the arrows between the points I and IV, and V and VI.

The readout of data from the logic element shall now be discussed in somewhat greater detail, also in connection with the hysteresis loop shown in fig. 7. Once more references to expressions such as logical 0 and logical 1 or "up" or "down" shall be avoided and there shall only be spoken of positive or negative polarization, represented respectively by the portion of the hysteresis loop which is located above the x axis and the portion of the hysteresis loop which is located below the x axis. If the logic element now is in a positive polarization state, represented by the point I on the hysteresis loop, the readout takes place by applying to the electrodes a voltage which preferably generates a field strength of about two times the coercivity field or more. The polarization of the logic element will hence move from the point I to III, provided that the read voltage has a positive sign. Due to the form of the hysteresis loop which in this case is very close to being square, a change of the polarization state from I to III will lead to a wholly insignificant charge transfer between the electrodes, and by the detection of charge transfer between the electrodes in the connected control circuit a very weak current signal will be obtained. If the logic element, however, is in a negative polarization state, represented by the point II on the hysteresis loop, the detected output current will by applying to the electrodes a positive voltage for the readout, first rise insignificantly and thereafter give a very sharply defined transient current pulse which represents the course between the points V and VI on the hysteresis loop where the charge transfer is large. Between the points I and II on the hysteresis loop the circumstance of a relatively flat hysteresis loop in other words will imply that the polarization only changes very little during the application of a positive voltage field, while the change during the application of a corresponding positive voltage when the logic memory element is at point II on the hysteresis loop will cause a very large

change of the polarization and particularly a substantial part of the change will take place between the points V and VI on the steepest portion of the hysteresis loop and also take place in a very short time period, something which results in the above-mentioned current transient as the detected output signal. This will also make it easy to discern in the readout between e.g. a logical 0 represented by the polarization state in the point I on the hysteresis loop and a logical 1 correspondingly represented by the point II on the hysteresis loop. The points III and IV on the hysteresis loop represent the saturation state for respectively the positive and the negative polarization, and when the applied electrical field is removed, the polarization will drift back respectively from III to I and from IV to II on the hysteresis loop. It shall, of course, be understood that in order to drive the polarization from I to III the field must according to the convention followed here be positive. while it for driving the polarization from state II to IV correspondingly, of course, must be negative.

Now it shall be remarked that the readout or the detection of the polarization state at II will be destructive, as the logic element after the readout arrives in a polarization state represented by the point III and thereafter drifts back to the stable state at I. If the readout of the polarization state took place when the logic element already was in I, this polarization state will, of course, be retained. After a readout of the data storage device based on ferroelectric memory cells according to the invention, information hence may be regarded as destructed by all memory cells in the storage device being in the same logical state, either 0 or 1. In practice, this of course, corresponds to an erasing of information and need not have negative consequences if the stored information only shall be read once or if readout only is required in a particular application. If the original information still shall be stored, it will, however, be necessary with a reset or refresh. This may take place by switching the logic element which originally was in the polarization state II but which after the readout will be in the polarization state I, back to the polarization state II by applying a negative voltage for the reset and preferably with the same field strength as in the readout. The polarisation will then take place along the hysteresis loop from I to IV. where the field is turned off and the logic elements drift back to the original polarization state at II. The reset of a logic element to the original polarization state after a readout, which destructed this state, can automatically take place by suitable verification and monitoring procedures implemented over the control circuits of the data

processing device and may for instance be software controlled according to a readout protocol. For instance there will in the reset of the polarization state at I to II, in other words in the switching of the polarization state I to the polarization state II, once more be output a current signal with a transient and this may then constitute the verification signal. Also a correct readout of the polarization state I may be verified either by applying to the logic element a voltage with opposite sign and reading a strong current signal, but the logic element will then be switched from I to II and must hence be reset. It will in other words quickly be realized that dependent on the initial polarization states and a possible destruction during the readout, the use of verification procedures and reset procedures will be interchangeable. In order to easier show this it may be referred to the accompanying table which discloses signs for the applied voltages during the respectively readout, verification and/or reset, as well as resulting currency pulses denoted as low or high according to whether the polarization state is changing along the loop from I to III, possibly from IV to II, or from I to IV, possibly from II to III.

The procedure for read-out of data as discussed herein is regarded in spite of the destruction as very advantageous when using ferroelectric materials with a nearly square hysteresis loop, as is the case for VDF-TFE as it gives a reliable detection and verification and the reset partly takes place spontaneously or in combination with verification. A pure small-signal detection, for instance between II and V, is in this case more problematic with regard to discrimination and requires an accurate control of the read voltage. If the hysteresis loop on the contrary has a more gentle course between II and V, and between V and VI, small signal detection may yet be used and reliable detection be obtained without reaching the saturation state III, while the absence of a sharp voltage threshold at V makes it easy to avoid a destructive read-out.

As already stated the form of the hysteresis loop which is dependent on the material, will be of importance for the response which is detected in a readout. As the hysteresis loop is depicted in fig. 7, it will be advantageous that the read voltage or the applied electric field which is used for detecting the polarization state is in the form of a threshold voltage, i.e. attains its maximum value immediately. Dependent of the polarization response and/or the time constant of the polarization it may be justified using a ramp voltage, i.e. a voltage which continuously increases to the desired maximum value which preferably will be twice the coercivity field or somewhat more.

Table. Preferred modes for readout, verification and reset, cf. fig. 7

	Readout			Verification			Reset			
							After readout		After verification	
	Voltage	Course	Current	Voltage	Course	Current	Voltage	Course	Voltage	Course
Initial positive polarization (I)	+	I→III	Low	-	I-IV	High	(none)	III→I (spontaneous)	+	IV→I, (IV→II, III→I spontaneous)
Initial negative polarization (II)	+	II→III	High	-	I-IV	High	= verification	III→II (III→I, IV→II spontaneous)	(none)	IV→II (spontaneous)

In a passively addressable electrode matrix displacement currents and resistive current components may be generated. These may mask a weak output signal in the current mode, such it will appear on detection of the polarization state I, while a transient signal as it is obtained by detection of the polarization state II, will be clearly discriminated because the displacement currents in common dielectric materials vary linearly with the field strength and appear instantly on application of the voltage, which also is the case of the resistive components. The resistive current components will further be present as long as the field is applied to the logic element. It will hence in every case be possible with a distinct discrimination to discern between the polarization state I or polarization state II. By the detection of the polarization state II on the hysteresis loop and the use of positive read voltage the polarization will move from II to III and the output current, the displacement current and the resistive current component will have a response as shown in fig. 8. The transient in the output current reaches a peak with a delay Δt after application of the read voltage and appears in a time window t_s which dependent on the sign of the field corresponds to one of the two steepest portions of the hysteresis loop of fig. 7. As will be seen, the current signal is distinctly discriminated relative to the displacement current and the resistive current component. The detection may take place by sampling or as a level comparison, for instance in the time window t_s which here for instance falls between V or VI on the hysteresis loop. The position of the time window on a time scale will depend on the polarization response for a given read voltage and the polarization properties of the ferroelectric material and the thin-film parameters.

Another interesting feature when using a ferroelectric material based on vinylidene fluoride/trifluoroethylene copolymers VDF-TFE is that their switching characteristics will depend on the electric field strength, i.e. the electrode voltage. Hence a high polarization voltage will influence the switching time of a logic element realized in the said ferroelectric material in such a manner that the higher the electric field strength the shorter the switching time. Typical switching characteristics for a vinylidene/trifluoroethylene copolymer are shown in fig. 9 which expresses the relationship between switching time and respectively the electrical flux density D and its derivative $\partial D/\partial \log t$ for different field strengths. It will be seen, as the coercivity field of this copolymer is about 40 MV/m, that a field strength of 100 MV/m, i.e. almost 2,5 times the coercivity fields, will result in a switching time of 10^{-5} s, while the switching time for field strength

insignificantly above that of the coercivity field, namely of 42 MV/m, gives a switching time of about 5s. The switching time is in other words reduced with 5 or 6 orders of magnitude with such an increase of the field strength. On the other hand it is for different reasons not desirable using a too high field strength, for one thing in order to avoid undesired stray capacitances or sneak currents in the matrix network and discharges through the thin film.

If the data processing device according to the invention is encumbered with impedance noise, it will be possible to provide current-amplifying line drivers connected to the logical elements in order to ensure noise immunity when driving for readout or switching. Such line drivers could possible be driven by the read/verification/reset voltage or over a separate supply line.

An embodiment of the data processing device according to the invention and corresponding to fig. 1 is shown in perspective in fig. 10, but with possible substrates and isolating layers removed. It appears in fig. 10 as a planar x,y electrode matrix and with the logic elements formed at each intersection between the electrodes 2;3 in the first and the second electrode structure. A planar matrix embodiment of this kind may be stacked layerwise in order to provide a volumetric data processing device with k stacked planar structures $S_1,...S_k$, as shown in fig. 11. It must then be provided layers 7 of electrical isolating material between each planar structure S which in section will appear roughly as shown in fig. 11. The electrodes 2.3 may be connected to not shown addressing and detection lines, i.e. current and voltage buses, e.g. provided in a semiconductor device made for this purpose, along the side edges of the volumetric device, or if the device is integrated as a hybrid device on silicon substrates, conveyed directly to drive voltage and control signal lines connected with driver and control units implemented in the silicon substrate in a compatible semiconductor technology. Addressing and detection may for instance take place in time multiplex or by using a logic addressing of each individual logic element. The number of logic addresses will then be the product of the number of stacked matrix structures or layers, the number of rows and the number of columns in each matrix structure. The number of separate addresses will be the sum of the number of x and y electrodes in a layer S and the number of layers $S_1,...S_k$ in the device. The combination of time multiplex-based and logic addressing may besides be used in order to realize a massive parallel addressing which could provide very high write and read speeds. In this regard reference may also be made to the discussion of

volumetrically implemented data processing devices as they for instance are disclosed in International patent application PCT/NO97/00154 of the present applicant, or the discussion of the stacked electrode devices as they are disclosed in Norwegian patent application 972803 of the present applicant. It will be obvious to persons skilled in the art that the logic elements realized either as bistable switches or memory cells may be used to configure logic gates or be included as switches in processor networks and arithmetic registers, possibly integrated with the logic elements realized as memory modules, or that the logic elements all are realized as memory cells, such that the device in fig. 11 will be a volumetric data device with high storage density. With the use of ferroelectric thin films it will be possible to achieve film thicknesses in the range of about 100 nm and corresponding electrode dimensions, something which implies that the voltages in order to generate the necessary field strengths will be in the range of about 10 volt. On one μm^2 it will then be possible to realize about 100 logic elements or memory cells, something which will imply a substantial improvement of the data storage density when compared to data storage devices of the ROM or RAM types based on conventional semiconductor technology.

PATENT CLAIMS

1. A ferroelectric data processing device, particularly for processing and/or storage of data with active or passive electrical addressing, comprising a data-carrying medium in the form of a thin film (1) of ferroelectric material, wherein the ferroelectric material by an applied electric field may attain a first or a second polarization state by being switched from a disordered state to one of the polarization states or from the first to the second polarization state or vice versa, wherein the ferroelectric material comprises logic elements (4), and wherein a polarization state assigned to a logic element (4) represents a logical value of the logic element, characterized in that the ferroelectric thin film (1) is provided as a continuous layer in or adjacent to respectively a first and second electrode structure, that the first and the second electrode structure each comprises substantially mutually parallel strip-like electrodes (2;3), such that the electrode structures mutually form a substantially orthogonal x,y matrix, wherein the electrodes (2) in the first electrode structure constitute the columns of the electrode matrix or the x electrodes and the electrodes (3) in the second electrode structure the rows of the electrode matrix or y electrodes, and that a portion of the ferroelectric thin film (1) at the intersection between an x electrode (2) and a y electrode (3) of the electrode matrix forms a logic element (4) such that the logic elements (4) jointly form an electrically connected passive matrix in the data processing device (2).

2. Data processing device according to claim 1, characterized in that a logic element (4) forms a bistabile switch in a data processor means.

3. Data processing device according to claim 1, characterized in that a logic element (4) forms a memory cell in a data storage means.

4. Data processing device according to claim 1, characterized in that the electrode structures and the ferroelectric thin film (1) are provided on a substrate.

5. Data processing device according to claim 1, characterized in that the ferroelectric thin film (1) is formed of a ceramic material.

6. Data processing device according to claim 1, characterized in that the ferroelectric thin film is formed of a ferroelectric liquid crystal material.

7. Data processing device according to claim 1, characterized in that the ferroelectric thin film (1) is formed of a polymer or copolymer.

8. Data processing device according to claim 1, characterized in that the copolymer is a vinylidene trifluoride/trifluoroethylene copolymer.

9. Data processing device according to claim 1, characterized in that the ferroelectric thin film (1) is provided between the first and the second electrode structure, and that the logic element (4) is formed in the intersection between an x electrode (2) and a y electrode (3).

10. Data processing device according to claim 1, characterized in that a layer (6) of an electrical isolating material is provided between and adjacent to the electrodes (2;3) of the first and the second electrode structure, that the ferroelectric thin film (1) is provided in the form of a continuous layer over the electrode structures on one side thereof, and that the logic elements (4) are formed respectively in a portion of the ferroelectric thin film (1) at the side edges of an y electrode (3) at the intersection between the x electrode (2) and the y electrode (3).

11. A method for manufacturing of a ferroelectric data processing device according to claim 10, characterized by successive steps for depositing a first electrode structure on a substrate, depositing a layer (6) of electrical isolating material over the first electrode structure, depositing a second electrode structure over the isolating layer (6), removing the isolating layer (6) where it is not covered by the second electrode structure, such that the electrodes (2) in the first electrode structure is exposed except in the intersection between the electrodes (2;3) of respectively the first and the second electrode structure, and depositing a ferroelectric thin film (1) in the form of a continuous layer over the electrode structures.

12. A method according to claim 11, characterized by the substrate being formed of a crystalline, polycrystalline or amorphous semiconductor material, for instance silicon.

13. A method according to claim 11, characterized by depositing a continuous layer of an electrical isolating material between the substrate and the first electrode structure before depositing the first electrode structure on the substrate.

14. A method for addressing of logic elements (4) in a ferroelectric data processing device, wherein the logic elements are provided in an electrically connected passive matrix, particularly for processing and/or storage of data with active or passive electrical addressing, depending on whether an addressing operation causes a change in a polarization state possibly already present in the logic element, comprising a data-carrying medium in the form of a thin film (1) of a ferroelectric material, wherein the ferroelectric thin film (1) by an applied electrical field may attain a first or second polarization state and is switched from a disordered state to one of the polarization states or from the first to the second polarization state or vice versa, wherein the ferroelectric thin film (1) is provided as a continuous layer in or adjacent to respectively a first or second electrode structure and comprises the logic elements (4) which contact electrodes (2;3) in this first and second electrode structure, wherein a polarization state assigned to a logic element (4) represents the logical value of the logic element, and wherein the addressing comprises steps for writing, reading, erasing and switching of data in the logic element, characterized by the step for writing comprising applying a voltage to the logic element and polarizing the ferroelectric thin film of the logic element (4) to a positive or a negative polarization state which respectively corresponds to a logical 0 or a logical 1 or vice versa, by the step for reading comprising applying a voltage to a logic element (4) and detecting the charge transfer between the electrodes (2;3) in the logic element in the form of a current value, which uniquely indicates the logical value, by the step for erasing comprising applying to all logic elements (4) in the data processing device a voltage which gives all logic elements one and the same polarization state, and by the step for switching of a logic element (4) from a polarization state which corresponds to a logical 0 or a logical 1 or vice versa, comprising applying a voltage to the logic element (4) which reverses the initial polarization state of the logic element.

15. A method according to claim 14,
characterized by applying a voltage which between the electrodes (2, 3) of the logic element (4) generates a field strength which is more than twice the coercivity field of the ferroelectric material.

16. A method according to claim 14, characterized by generating the applied voltage as a ramp voltage.

17. A method according to claim 14, characterized by generating the applied voltage as a threshold voltage.

18. A method according to claim 14, characterized by the current detection in the reading step taking place by sampling in the time domain.

19. A method according to claim 14, characterized by the current detection in the reading step taking place in a time window dependent on the saturation time constant of the polarization.

20. A method according to claim 18 or 19, characterized by the current detection taking place by a level comparison.

21. A method according to claim 14, characterized by verifying the current detection in the step for reading in an immediate following step by applying to the logic element (4) a voltage corresponding to the voltage used in the reading step, but of opposite polarity, and detecting the charge transfer between the electrodes (2;3) in the logic element (4) in the form of a current value.

22. A method according to claim 14 or claim 21, wherein the step for reading and/or verification causes a destruction of a datum stored in the logic element (4), characterized by the logic element (4) being reset to its initial logic state after the current detection in the step for reading or verification by applying to the logic element a voltage which restores the initial polarization state of the logic element.

23. A method according to claim 22, characterized by the reset of the logic element (4) taking place in combination with the step for verification and itself being verified in a further current detection.

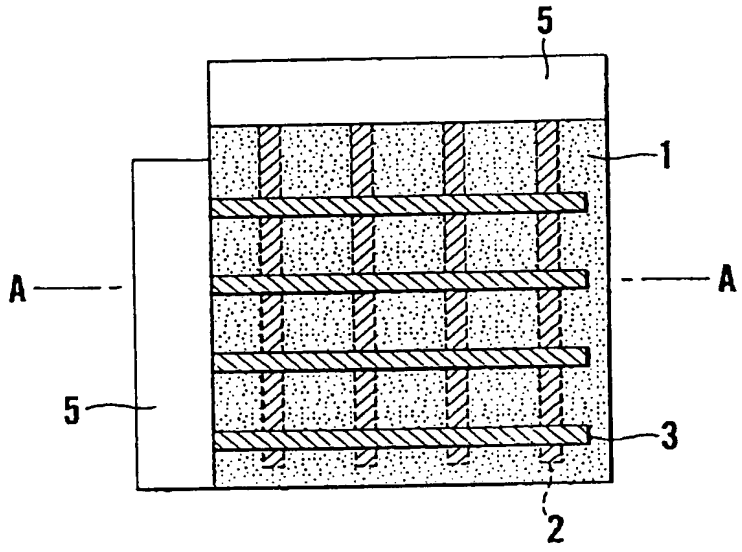


Fig.1

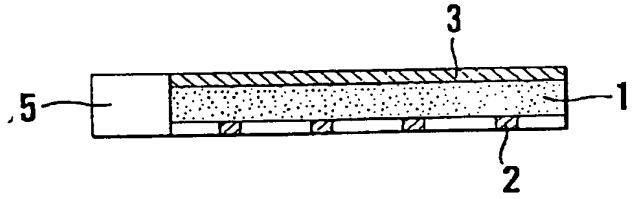


Fig.2

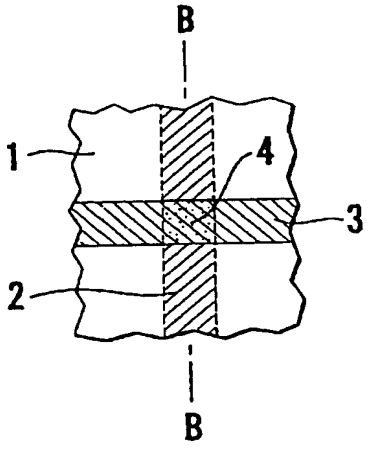


Fig.3a

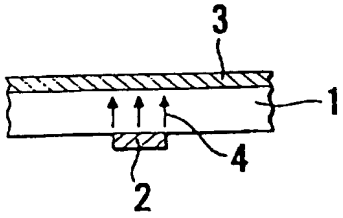


Fig.3b

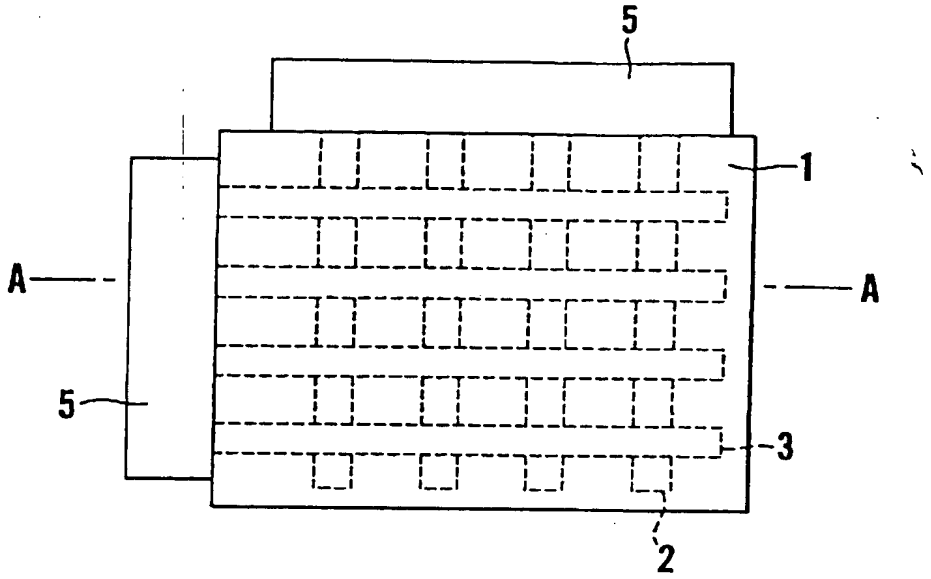


Fig.4

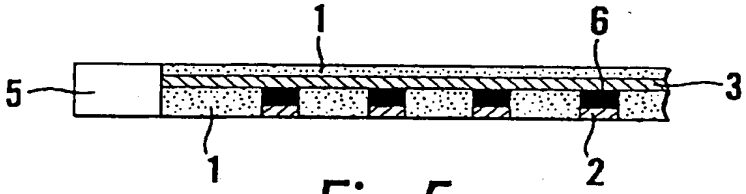


Fig.5

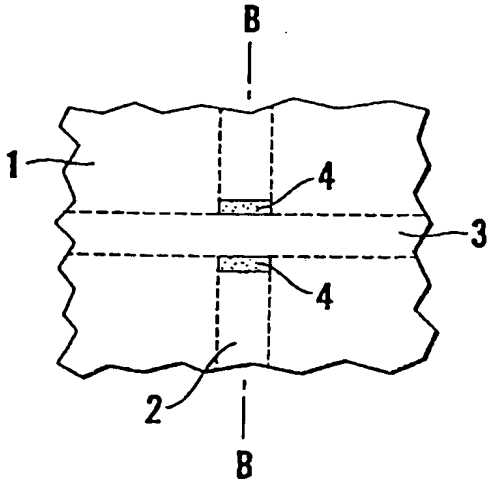


Fig.6a

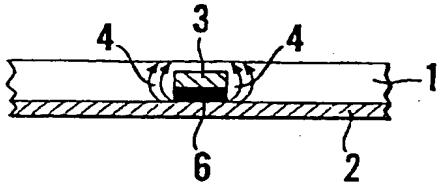
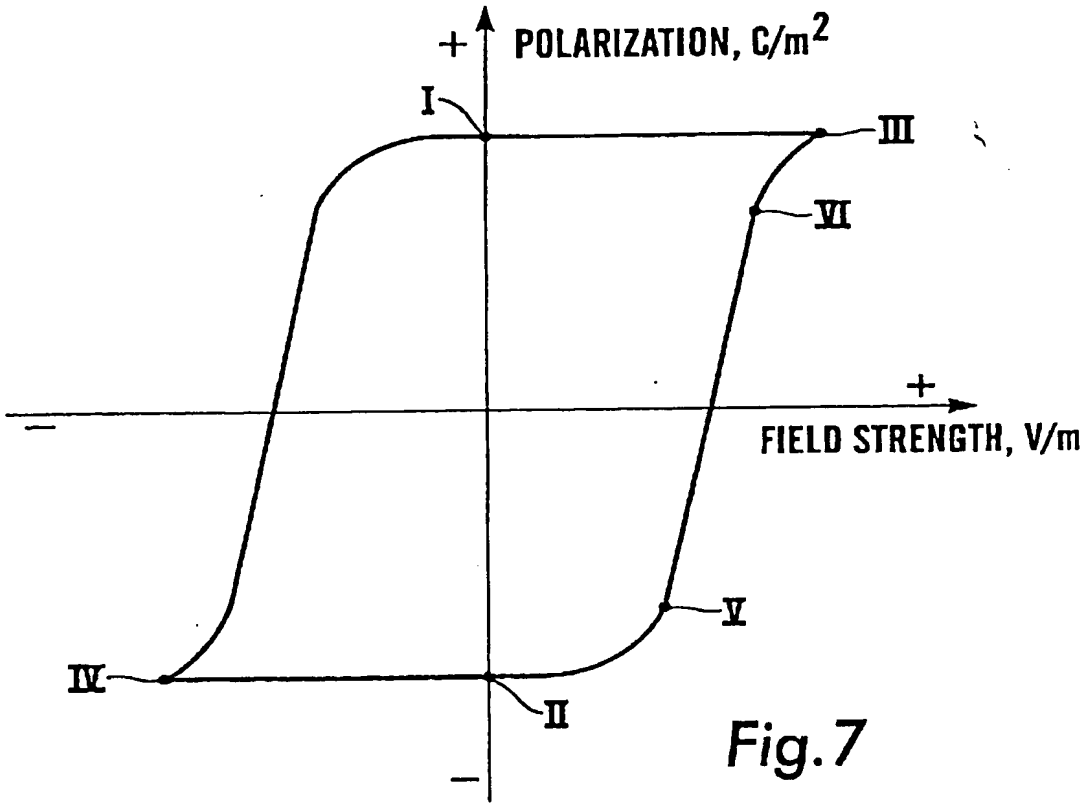


Fig.6b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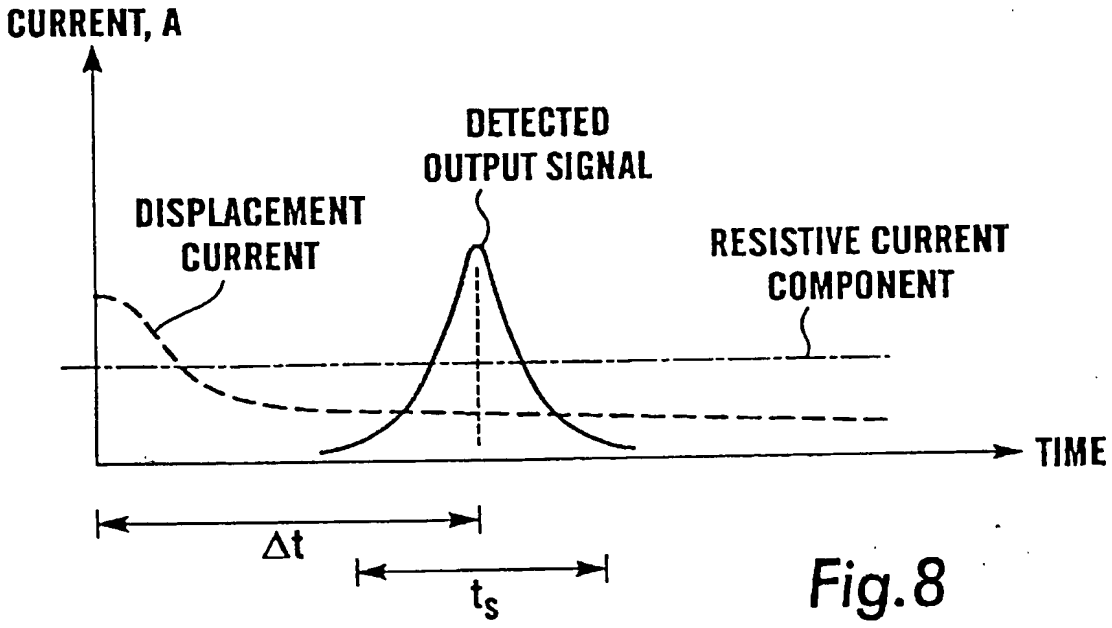
I
III
VI
+
FIELD STRENGTH, V/m
—
V
IV
II
—

Fig.7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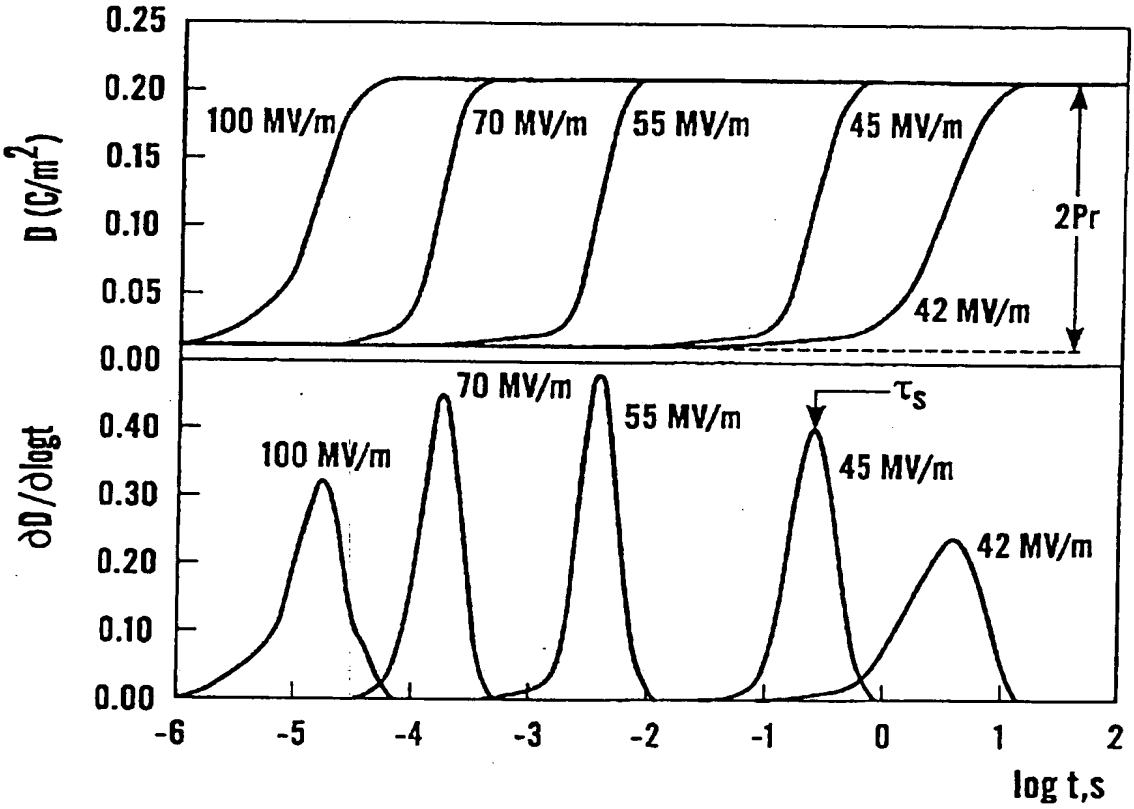
OUTPUT SIGNAL
DISPLACEMENT
CURRENT
RESISTIVE CURRENT
COMPONENT
TIME
Δt
ts

Fig.8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0.20
0.15
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0.05
0.00
D (C/m²)
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70 MV/m
55 MV/m
45 MV/m
42 MV/m
2Pr
0.40
0.30
0.20
0.10
0.00
∂D/∂logt
100 MV/m
70 MV/m
55 MV/m
45 MV/m
42 MV/m
τs
-6
-5
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-2
-1
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1
2
log t,s

Fig.9

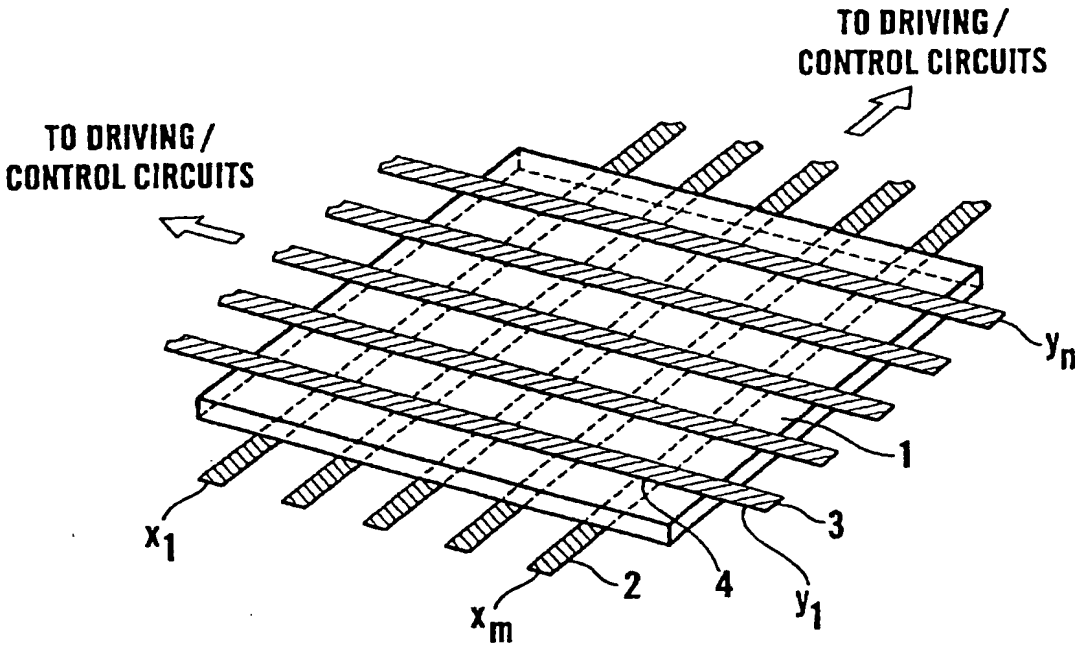
TO DRIVING / CONTROL CIRCUITS
TO DRIVING / CONTROL CIRCUITS
y_n
1
3
x_1
2
4
y_1
x_m

Fig. 10

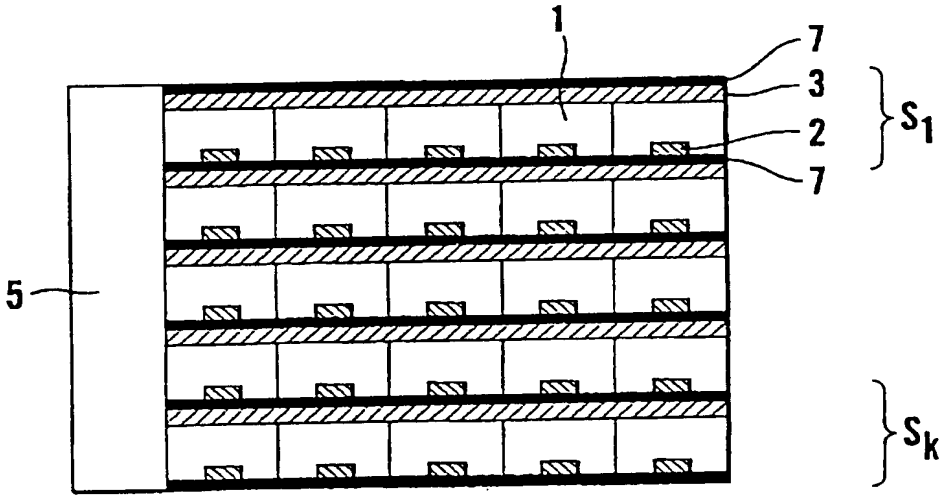
1
7
3
2
7
S_1
5
S_k

Fig. 11

INTERNATIONAL SEARCH REPORT

International application No.
PCT/NO 98/00237

A. CLASSIFICATION OF SUBJECT MATTER

IPC6: G11C 11/22, H03K 19/185
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC6: G11C, H03K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

SE,DK,FI,NO classes as above

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EDOC, WPIL, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5329485 A (YASUO ISONO ET AL), 12 July 1994 (12.07.94), column 9, line 25 - column 14, line 13, claim 1	1-5,9,14,17, 22
Y	--	16,18-21,23
X	US 5375085 A (BRUCE E. GNADE ET AL), 20 December 1994 (20.12.94), column 3, line 18 - column 5, line 36	1-5,9,14
Y	--	6

[X] Further documents are listed in the continuation of Box C. [X] See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
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"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance: the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance: the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search
17 February 1999

Date of mailing of the international search report
22 -02- 1999

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/NO 98/00237

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	IBM Technical Disclosure Bulletin, Volume 37, No 11, November 1994, -, "Ultrafast Nonvolatile Ferroelectric Information Storage Device" page 421 - page 424	1-4,7-9
X	Patent Abstracts of Japan, Vol 17,No 477, P-1603 abstract of JP 5-114284 A (OLYMPUS OPTICAL CO LTD), 7 May 1993 (07.05.93)	1-4,9,14,17
A		18-23
X	Patent Abstracts of Japan, abstract of JP 6-131866 A (OLYMPUS OPTICAL CO LTD), 13 May 1994 (13.05.94)	1-4,9,14
Y		16,18-21,23
X	Patent Abstracts of Japan, Vol 10,No 209, E-421 abstract of JP 61-48983 A (TORAY IND INC), 10 March 1986 (10.03.86)	1-4,7-9
Y	US 5500749 A (YUTAKA INABA ET AL), 19 March 1996 (19.03.96), column 7, line 33 - column 8, line 26	6

INTERNATIONAL SEARCH REPORT

Information on patent family members

02/02/99

International application No.
PCT/NO 98/00237

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		US 5487031 A	23/01/96
US 5500749 A	19/03/96	US 5805129 A	08/09/98
		EP 0494626 A	15/07/92
		JP 2802685 B	24/09/98
		JP 4251218 A	07/09/92